lines. As shown in FIG. 4, the horizontal portion **26(a)** can cover a majority of the upper surface of the semiconductor die **30**. An area **30(b)** of the semiconductor die **30** under the horizontal portion **26(a)** of the bus member **26** can include source regions. An exposed area **30(a)** to a side of the horizontal portion **26(a)** and that is not covered by the bus member **26** can have connections to a gate.

IN THE CLAIMS:

The claims have been amended as follows.

1. (Amended) A semiconductor die package comprising:

a semiconductor die comprising a vertical power transistor, wherein the semiconductor die has a first surface and a second surface;

a source region at the first surface of the semiconductor die;

a gate at the first surface of the semiconductor die;

a drain region at the second surface of the semiconductor die;

a ground plane proximate the second surface and distal to the first surface; and

a bus member covering a portion of the first surface of the semiconductor die and having at least one leg, wherein the bus member electrically couples the source region of the semiconductor die to the ground plane.

2. (Unamended) The semiconductor die package of claim 1 wherein the vertical power transistor is a vertical diffused metal oxide semiconductor (VDMOS).

3. (Unamended) The semiconductor die package of claim 1 further comprising:

an isolator layer between the ground plane and the semiconductor die.

4. (Unamended) The semiconductor die package of claim 1 further comprising:

an isolator layer between the ground plane and the semiconductor die; and

a conductive layer between the isolator layer and the semiconductor die.

5. (Unamended) The semiconductor die package of claim 1 further comprising:

an isolator layer between the ground plane and the semiconductor die;

a conductive layer between the isolator layer and the semiconductor die; and

a ceramic carrier enclosing the semiconductor die, the bus member, the isolator layer, and the conductive layer.

6. (Unamended) The semiconductor die package of claim 1 wherein the vertical power transistor is a vertical diffused metal oxide semiconductor (VDMOS) RF power transistor.

7. (Unamended) The semiconductor die package of claim 1 further comprising:

an isolator layer between the ground plane and the semiconductor die;

a conductive layer between the isolator layer and the semiconductor die;

a ceramic carrier enclosing the semiconductor die, the bus member, the isolator layer, and the conductive layer;

a drain lead passing through the ceramic carrier;

a first wire coupling the drain lead to the drain region via the conductive layer;

a gate lead passing through the ceramic carrier; and

a second wire coupling the gate lead to the gate.

8. (Unamended) The semiconductor die package of claim 1 further comprising a matching network electrically coupled to the gate.

9. (Unamended) The semiconductor die package of claim 1 further comprising:

an isolator layer between the ground plane and the semiconductor die;

a matching network on the isolator layer;

a conductive layer between the isolator layer and the semiconductor die;

a ceramic carrier enclosing the semiconductor die, the bus member, the isolator layer, and the conductive layer;

a drain lead passing through the ceramic carrier;

a first wire coupling the drain lead to the drain region via the conductive layer;

a gate lead passing through the ceramic carrier;

a second wire coupling the gate lead to the matching network; and

a third wire coupling the gate to the matching network.

10. (Amended) The semiconductor die of claim 1 wherein the gate is a trenched gate.

11. (Unamended) A semiconductor die package comprising:

a semiconductor die comprising a vertical power transistor, wherein the semiconductor die has a first surface and a second surface;

a source region at the first surface of the semiconductor die;

a gate at the first surface of the semiconductor die;

a drain region at the second surface of the semiconductor die;

a ground plane proximate the second surface and distal to the first surface;

a conductive layer between the ground plane and the semiconductor die;

an isolator layer disposed between the conductive layer and the ground plane;

a bus member covering a major portion of the first surface of the semiconductor die and electrically coupling the source region of the semiconductor die to the ground plane;

a carrier enclosing the semiconductor die and the bus member;

a drain lead passing through the carrier;

a first electrical conductor coupling the drain lead to the conductive layer and the drain region;

a gate lead passing through the carrier; and

a second electrical conductor coupling the gate lead to the gate.

12. (Unamended) The semiconductor die package of claim 11 wherein the bus member is a first bus member and wherein the first electrical conductor is a second bus member and the second electrical conductor is a third bus member, wherein the second and third bus members each have a pair of legs with different lengths.

13. (Unamended) The semiconductor die package of claim 11 wherein the vertical power transistor is a vertical diffused metal oxide semiconductor (VDMOS) RF power transistor.

14. (Unamended) The semiconductor die package of claim 11 further comprising:

a matching network coupled to the gate.

15. (Unamended) The semiconductor die of claim 11 wherein the bus member is a first bus member and wherein the first electrical conductor is a second bus member and the second electrical conductor is a third bus member, and wherein the first, second, and third bus members each have a horizontal portion and two legs that are perpendicular to the horizontal portion.

16. (Amended) A semiconductor die package comprising:

a semiconductor die comprising a vertical power transistor, wherein the semiconductor die has a first surface and a second surface;

an emitter region at the first surface of the semiconductor die;

a base region at the first surface of the semiconductor die;

a collector region at the second surface of the semiconductor die;

a ground plane proximate the second surface and distal to the first surface; and

a bus member covering a portion of the first surface of the semiconductor die and having at least one leg, wherein the bus member electrically couples the [source] emitter region of the semiconductor die to the ground plane.

17. (Unamended) The semiconductor die package of claim 16 wherein the bus member comprises two legs of substantially equal length.

18. (Amended) A semiconductor die package comprising:

a semiconductor die comprising a transistor, wherein the semiconductor die has a first surface and a second surface;

a source region in the semiconductor die;

a gate in the semiconductor die;

a drain region in the semiconductor die;

a ground plane proximate the second surface and distal to the first surface; and

a bus member covering a portion of the first surface of the semiconductor die and having at least one leg, wherein the bus member electrically couples the source region of the semiconductor die to the ground plane.

19. (Unamended) The semiconductor die package of claim 18 wherein the source region, the gate, and the drain region are at the first surface of the semiconductor die.